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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,119	10/21/2003	Clayton Gibbs	TI-34137	3655

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EXAMINER	
FRANKLIN, RICHARD B	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,119	GIBBS ET AL.	
	Examiner	Art Unit	
	Richard Franklin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 9 have been examined.

Response to Arguments

2. Applicant's arguments, see pages 8 – 11, filed 22 November 2005, with respect to claims 1 – 4 and 9 have been fully considered and are persuasive. The rejections of claims 1 – 4 and 9 have been withdrawn.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1 – 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 1 recites the limitation "the change of state" in line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim.

The Examiner has interpreted the limitation as reciting "a change of state."

5. Claim 1 recites the limitation "the occurrence of" in line 4 of the claim. There is insufficient antecedent basis for this limitation in the claim.

The Examiner has interpreted the limitation as reciting "an occurrence of."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 – 2, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Microcontroller Technology: The 68HC11 by Peter Spasov (hereinafter Spasov) in view of Bolt et al. US Patent No. 4,769,769 (hereinafter Bolt).

As per claim 1, Spasov teaches triggering a burst transfer from a change of state of a FIFO output signal, the change of state being the occurrence of a triggering event within the FIFO device (Spasov; Page 253, Section "The First In, First Out (FIFO) Queue, Paragraphs 2 and 3).

Spasov does not teach inhibiting triggering any further transfers until a current transfer is complete.

Bolt teaches inhibiting triggering any further transfers until a current transfer is complete (Bolt; Col 2 Lines 36 – 40).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Spasov to include trigger inhibiting because doing so allows for synchronization in a conflict-free manner for supplying and fetching data (Bolt; Col 10 Lines 40 – 42).

As per claim 2, Spasov further teaches wherein the triggering event is an indication of the fullness of the FIFO (Spasov; Page 253, Section "The First In, First Out (FIFO) Queue, Paragraphs 2 and 3).

As per claim 5, Spasov teaches wherein the burst transfer includes transfer of predetermined amount of data in fixed number of sequential clock cycles because transferring a set amount of data without interruption is a property of burst transfers (Spasov; Page 253, Section "The First In, First Out (FIFO) Queue, Paragraphs 2 and 3).

7. Claims 3 – 4, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Microcontroller Technology: The 68HC11 by Peter Spasov (hereinafter Spasov) in view of Bolt et al. US Patent No. 4,769,769 (hereinafter Bolt) as applied to claims 1 – 2, and 5 above and further in view of Applicants Admitted Prior Art (hereinafter AAPA).

As per claim 3, Spasov in view of Bolt teach a triggering event that is a change in a FIFO fullness indicator flag (Spasov; Page 253, Section "The First In, First Out (FIFO) Queue, Paragraphs 2 and 3).

Spasov in view of Bolt does not teach wherein the FIFO fullness flag denotes the FIFO is less than or greater than half full; and the triggering event is changing from the FIFO fullness flag denoting less than half full to greater than half full.

AAPA teaches a conventional FIFO wherein the FIFO fullness flag denotes the FIFO is less than or greater than half full (AAPA; Background Section of Specification, Page 4 Lines 14 – 20); and the triggering event is changing from the FIFO fullness flag

denoting less than half full to greater than half full (AAPA; Background Section of Specification, Page 4 Lines 14 – 20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Spasov and Bolt to include the half full fullness flag because that flag is well known and typically used in FIFOs when systems are loosely coupled to the FIFO and perform burst transfers based on the status of the flag (AAPA; Background Section of Specification, Page 3 Lines 19 – 27).

As per claim 4, Spasov in view of Bolt teach a triggering event that is a change in a FIFO fullness indicator flag (Spasov; Page 253, Section "The First In, First Out (FIFO) Queue, Paragraphs 2 and 3).

Spasov in view of Bolt does not teach wherein the FIFO fullness flag denotes the FIFO is less than or greater than half full; and the triggering event is changing from the FIFO fullness flag denoting greater than half full to less than half full.

AAPA teaches a conventional FIFO wherein the FIFO fullness flag denotes the FIFO is less than or greater than half full (AAPA; Background Section of Specification, Page 4 Lines 14 – 20); and the triggering event is changing from the FIFO fullness flag denoting greater than half full to less than half full (AAPA; Background Section of Specification, Page 4 Lines 24 – 27).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Spasov and Bolt to

include the half full fullness flag because that flag is well known and typically used in FIFOs when systems are loosely coupled to the FIFO and perform burst transfers based on the status of the flag (AAPA; Background Section of Specification, Page 3 Lines 19 – 27).

As per claim 9, Spasov in view of Bolt teach inhibiting further burst transfers until the end of a current burst transfer (See rejection for claim 1).

Spasov in view of Bolt does not teach inhibiting further burst transfers until a predetermined number of clock cycles following the completion of a current burst transfer.

AAPA teaches in a conventional FIFO system, inhibiting further burst transfers until a predetermined number of clock cycles following the completion of a current burst transfer (AAPA; Background Section of Specification, Page 6 Lines 6 – 11).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Spasov and Bolt to include inhibiting further burst transfers until a predetermined number of clock cycles following the completion of a current burst transfer because doing so allows for accounting for synchronization delays within the FIFO (AAPA; Background Section of Specification, Page 6 Lines 9 – 11).

8. Claims 6 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Microcontroller Technology: The 68HC11 by Peter Spasov (hereinafter Spasov) in view

of Bolt et al. US Patent No. 4,769,769 (hereinafter Bolt) as applied to claims 1 – 2, and 5 above and further in view of Johnson US Patent Application Publication No. 2004/0010637 (hereinafter Johnson).

As per claim 6, Spasov in view of Bolt teaches a burst transfer of a predetermined amount (See rejection for claim 5).

Spasov in view of Bolt does not teach wherein the predetermined amount of data in the burst transfer is set by an input to the FIFO device from the processor device during initialization.

Johnson teaches wherein the predetermined amount of data in the burst transfer is set by an input to the FIFO device from the processor device during initialization (Johnson; Figure 1 Items 100 and 110, Paragraphs [0005] – [0007]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Spasov and Bolt because setting the predetermined amount of data in a burst transfer by an input to the FIFO device allows for different sizes of burst transfers to take place in the device without the need to use extra clock cycles (Johnson; Paragraph [0006]).

As per claim 7, Spasov in view of Bolt teaches a burst transfer of a predetermined amount (See rejection for claim 5).

Spasov in view of Bolt does not teach wherein the predetermined amount of data in a burst transfer is set by an input to a programmable FIFO device register.

Johnson teaches wherein the predetermined amount of data is in a burst transfer is set by an input to a programmable FIFO device register (Johnson; Figure 1 Items 100 and 110, Paragraphs [0005] – [0007]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Spasov and Bolt because setting the predetermined amount of data in a burst transfer by a programmable FIFO device register allows for different sizes of burst transfers to take place in the device without the need to use extra clock cycles (Johnson; Paragraph [0006]).

As per claim 8, Johnson further teaches wherein the processor device supplies the predetermined amount of data to the programmable FIFO device register's input pins (Johnson; Paragraphs [0022] – [0023]).

Johnson does not explicitly teach wherein the processor device supplies the predetermined amount of data to the programmable FIFO device register via an output pin. However, it would have been obvious to one of ordinary skill in the art that the input pins of the FIFO device register are connected to output pins of the of the processor device because in order to supply the data to the register's input pins, the processor device has to supply the data to its output pins.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Richard Franklin
Patent Examiner
Art Unit 2181

KIM HUYNH
SUPERVISORY PATENT EXAMINER
2/2/06